

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

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In re Patent issued to:  
Villarosa et al.

Patent No.: 6,879,650

Application No.: 09/353,120

Issued: April 12, 2005

Filed: July 14, 1999

Title: Circuit and method for detecting and correcting  
data clocking errors.

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**STATEMENT UNDER 3.73(b)**

Advent IP LLC states that it is the assignee of the entire interest of the patent identified above by virtue of a chain of title from the inventors, of the patent identified above, to the current assignee as follows:

1. From **Louis S. Vilarrosa, Jr. and Mark D. Studebaker** to **Paradyne Corporation**  
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Reel **010106** Frame **0783**
2. From **Paradyne Corporation** to **Verso Technologies, Inc.**  
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3. From **Verso Technologies, Inc.** to **Advent IP LLC**  
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Reel **022343** Frame **0807**

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

Dated: March 12, 2009

Respectfully submitted,  
Signature: /Benzion Wachsman/  
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Title: General Manager